

PROLABS – XLDACBLx-C

QSFP+ to QSFP+ 40G Copper Cable Assembly

Overview

PROLABS's QSFP+ (Quad Small Form-factor Pluggable Plus) Copper direct-attach cables are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP+ ports. QSFP+ are designed for a high density cabling interconnect system capable of delivering an aggregate data bandwidth of 40Gbps. This interconnect system is fully compliant with QSFP+ MSA. The QSFP+ cables support the bandwidth transmission requirements as defined by IEEE802.3ba(40Gbps) .

Product Features

- Up to 40 GBd bi-directional data links
- Compliant with QSFP+ MSA specifications
- Fully Compliant with IEEE802.3ba and Infiniband QDR specifications
- 4 independent duplex channels operating at 10Gbps,also support for 2.5Gbps,5Gbps data rates
- AC coupled inputs and outputs
- 100 Ohm differential impedance
- All-metal housing for superior EMI performance
- Single power supply 3.3V, low power consumption
- RoHS Compliance
- Operating temperature range: 0°C to 70°C .

Applications

- 40Gigabit Ethernet
- Serial Data Transmission

Ordering Information

Part Number	Description
XLDACBL1-C	40G QSFP+ Direct Attach Copper Cable Assembly, 1 Meter
XLDACBL3-C	40G QSFP+ Direct Attach Copper Cable Assembly, 3 Meter
XLDACBL5-C	40G QSFP+ Direct Attach Copper Cable Assembly, 5 Meter

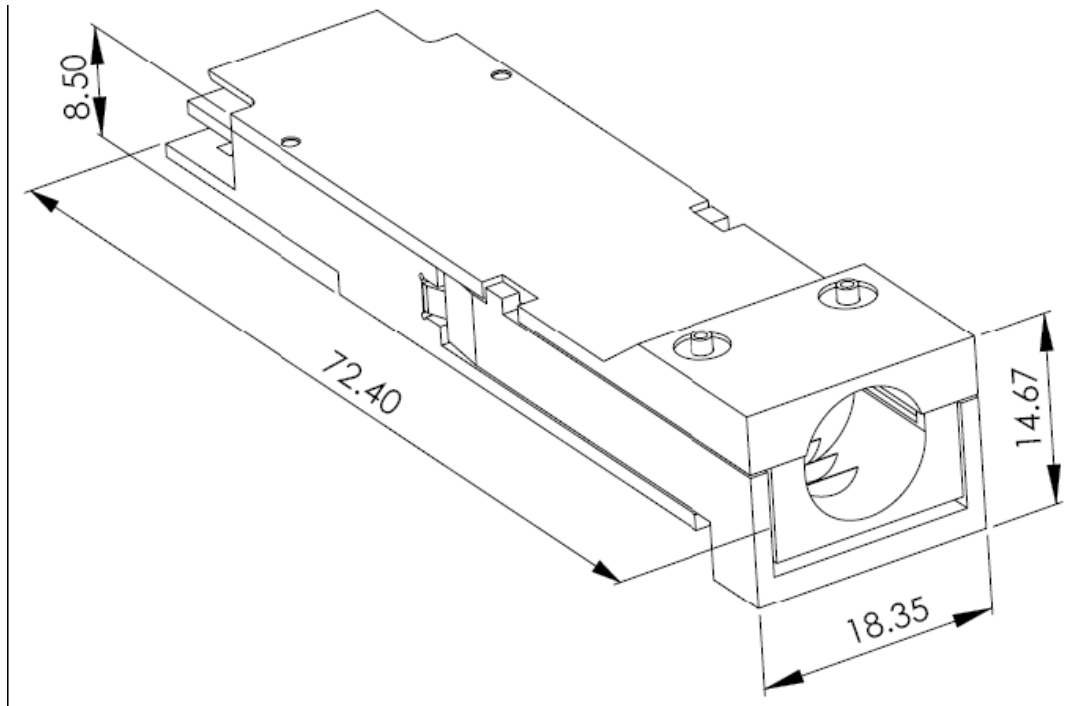
General Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Bit Error Rate	<i>BER</i>			10^{-12}		
Operating Temperature	<i>T_{OP}</i>	0		70	°C	Case temperature
Storage Temperature	<i>T_{STO}</i>	- 40		85	°C	Ambient temperature
Input Voltage	<i>V_{CC}</i>	3	3.3	3.6	V	
Maximum Voltage	<i>V_{MAX}</i>	- 0.5		4	V	For electrical power interface

Cable Mechanical Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Wire Gauge		24AWG		30AWG		
Cable Impedance	<i>Z</i>	95	100	105	Ohm	

QSFP+ Outline Dimensions

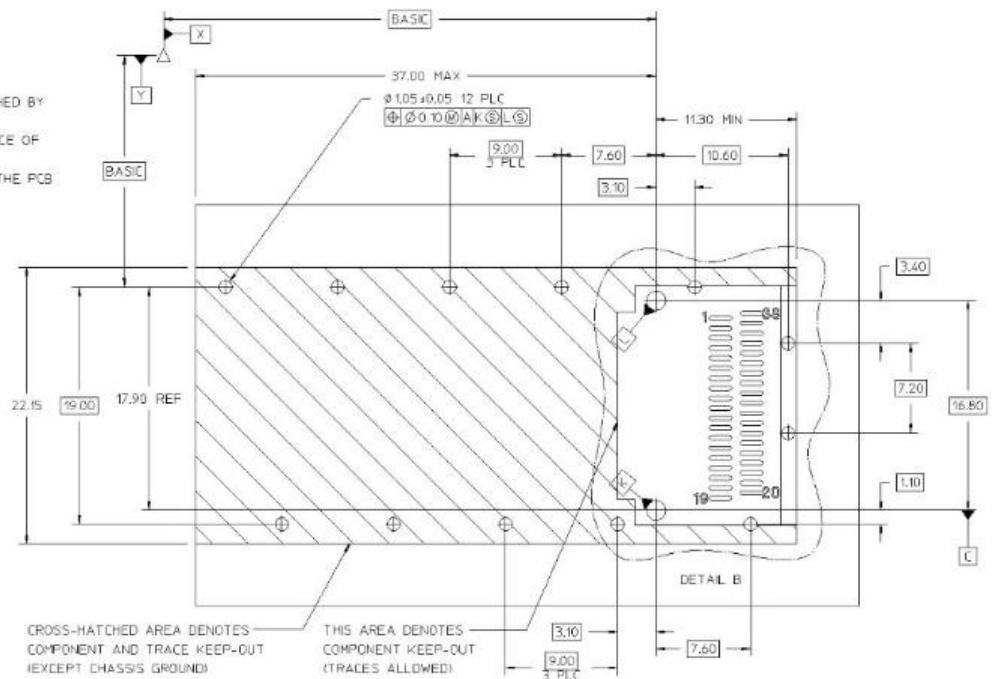


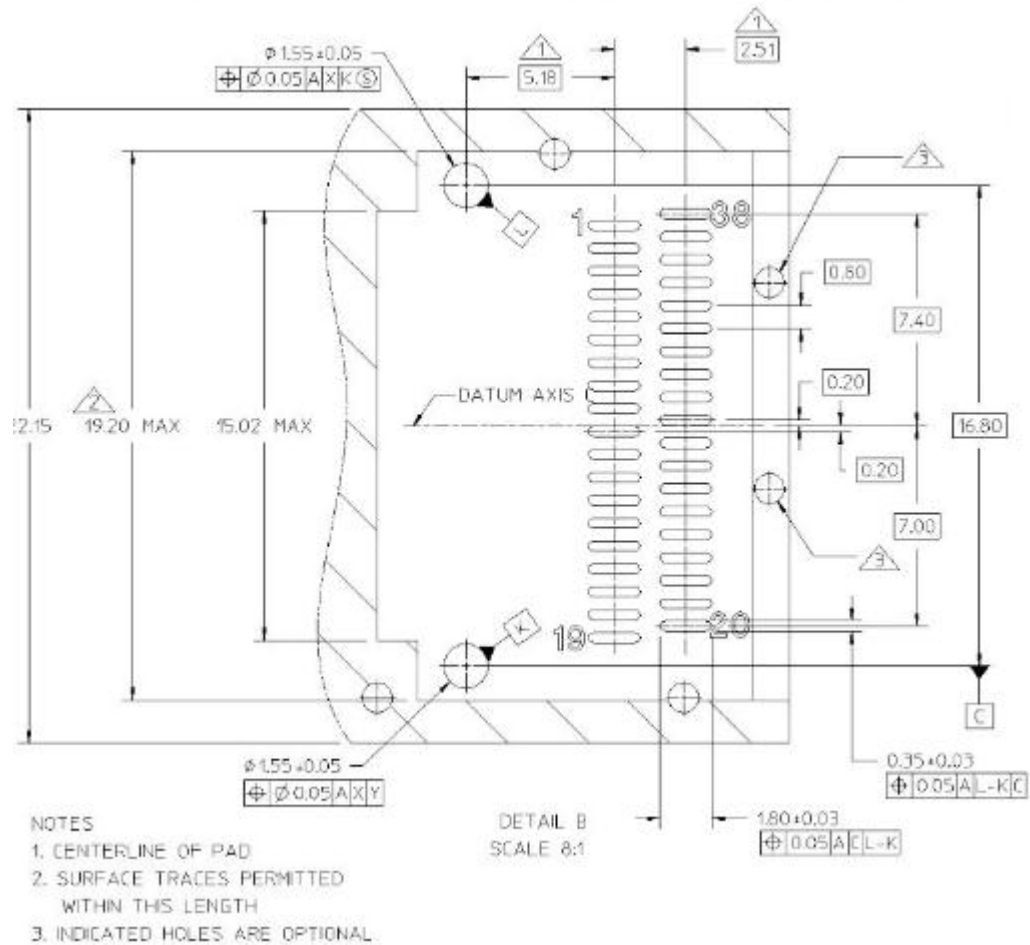
**ALL DIMENSIONS ARE $\pm 0.2\text{mm}$ UNLESS OTHERWISE SPECIFIED
UNIT: mm**

PCB Layout Recommendation

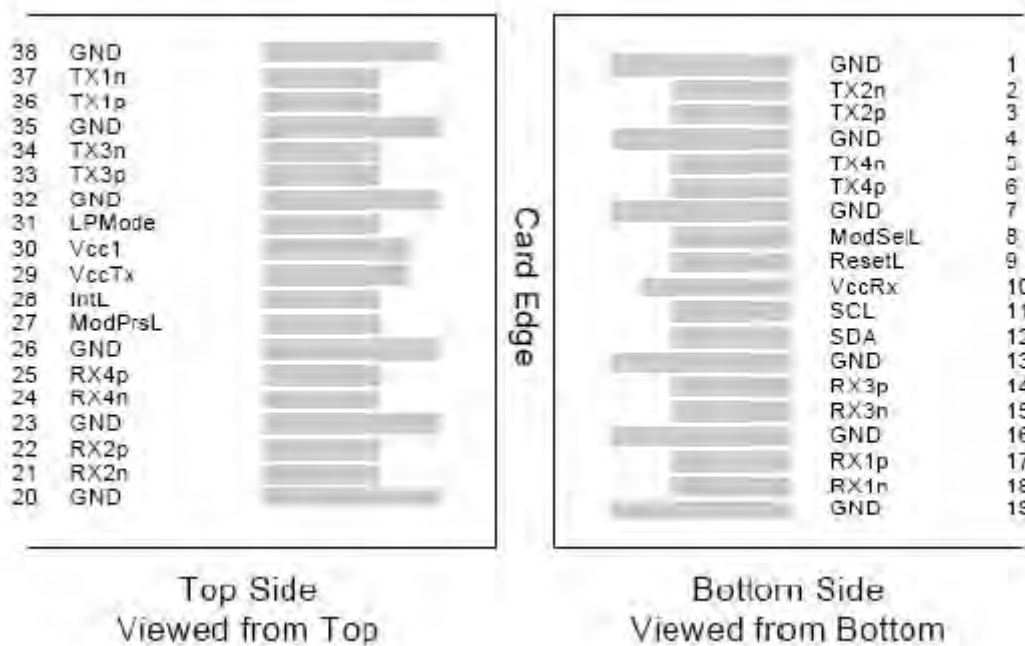
NOTES

1. DATUM X & Y ARE ESTABLISHED BY THE CUSTOMER'S FIDUCIAL
2. DATUM A IS THE TOP SURFACE OF THE HOST BOARD
3. LOCATION OF THE EDGE OF THE PCB IS APPLICATION SPECIFIC
4. FINISHED PTH HOLE SIZE





Electrical Pad Layout



Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V _{cc} RX	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	V _{cc} TX	+3.3V Power Supply transmitter	
30	V _{cc1}	+3.3V Power Supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	

References

1. IEEE standard 802.3ba. IEEE Standard Department.
2. QSFP+ 10 Gbs 4X PLUGGABLE TRANSCEIVER –SFF-8436