

## **PROLABS – XLAOCBLx-C**

### **40GBd QSFP+ Active Optical Cable Transceiver**

#### **XLAOCBLX-C Overview**

PROLABS's XLAOCBLX-C QSFP+ active optical cable transceivers are 4-channel active optical cable for QSFP+ applications that is designed to meet the QSFP+ 10GBPS X 4 Pluggable Transceiver SFF-8436 specification. This full-duplex optical assembly offers 4 independent transmit and receive channels, each capable of 10Gbps for an aggregate bandwidth of 40Gbps.

The cables use the standard multimode fiber cable carrying a nominal wavelength of 850nm. The electrical interface is standard 38 contact edge type connector and is electrically compliant with the SFI+ and PPI interface supporting Infiniband, Ethernet, Fiber Channel. The connector is hot pluggable and provides I2C serials access via an on-board microcontroller.

QSFP+ AOC can be used as a direct replacement for traditional copper cables with the added benefit of a lighter weight and smaller diameter solution for cable lengths from 1 to 100 meters.

#### **Product Features**

- 4 high-speed full duplex channels
- QSFP+ MSA compliant
- Cable lengths from 1 to 100 meters
- Small 3mm diameter fiber cable
- Low Power consumption, less than 1W
- RoHS Compliance
- Operating temperature range: 0°C to 70°C.

#### **Applications**

- 40G Ethernet
- Infiniband interconnects

#### **Ordering Information**

<i><b>Part Number</b></i>	<i><b>Description</b></i>
XLAOCBLx-C	40G QSFP+ Active optical Cable (length from 1m to 100m)

## General Specifications

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Bit Error Rate	BER			$10^{-15}$		
Operating Temperature	T <sub>OP</sub>	0		70	°C	Case temperature
Storage Temperature	T <sub>STO</sub>	-40		85	°C	Ambient temperature
Input Voltage	V <sub>CC</sub>	3.14	3.3	3.47	V	
Maximum Voltage	V <sub>MAX</sub>	-0.5		3.6	V	For electrical power interface

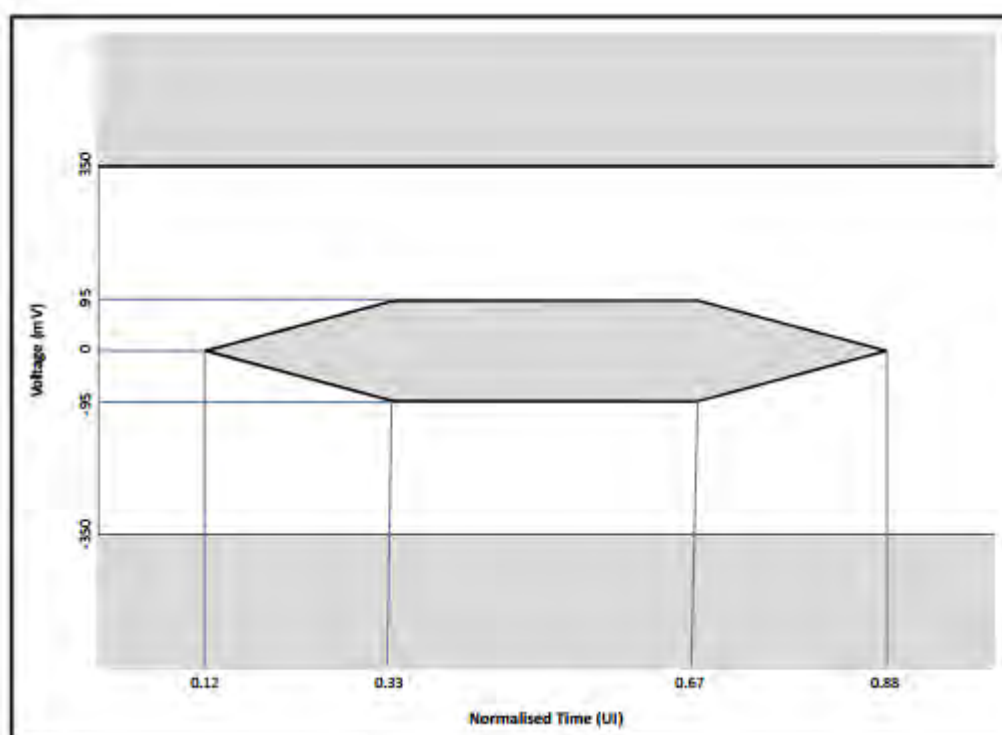
## Link Distances

<i>Parameter</i>	<i>Fiber Type</i>	<i>Distance Range (m)</i>
40 GBd	MMF	Up to 100

## AOC Electrical Input Requirements

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Data Rate Per Channel	Dr		0.001	10.5	GB/s	Non condensing
Differential Input Amplitude	V <sub>IN_PP</sub>	150		1600	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
AC Common Mode Voltage	V <sub>cm</sub>	15			mV	
Total Jitter	T <sub>J</sub>			0.28	UIp-p	
Data Dependent Jitter	DDJ			0.1	UIp-p	
Eye Mask			See note			

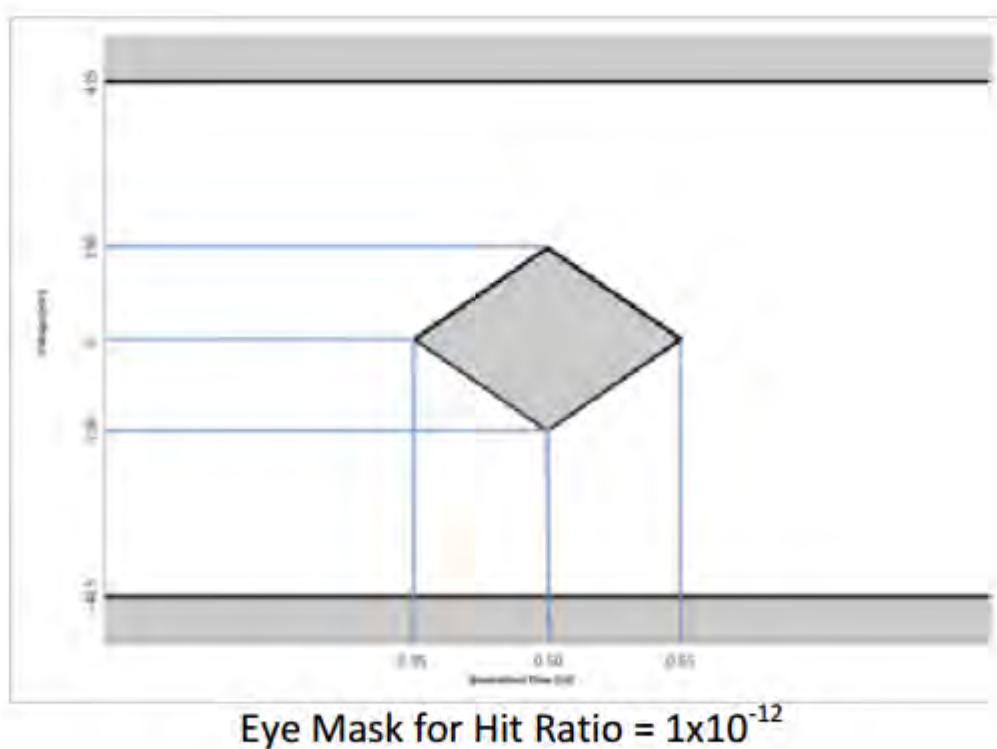
Note: The worst case electrical input is defined by the eye mask:



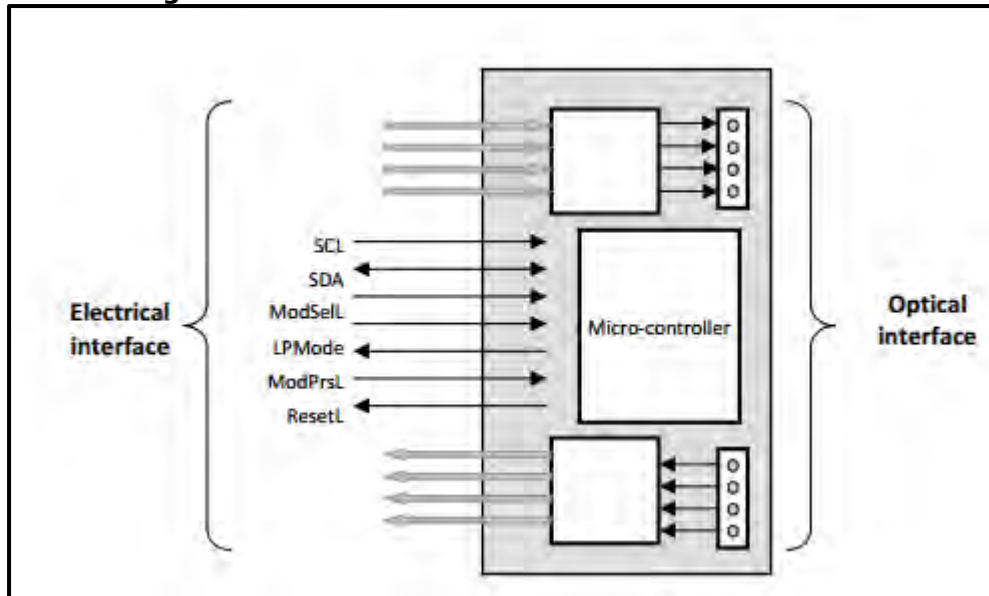
## AOC Electrical Output Requirements

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Data Rate Per Channel	Dr		0.001	10.5	GB/s	Non condensing
Differential Output Amplitude	Vout_PP	340		700	mV	
Differential Output Amplitude in Squelched state	Vout_sq			50	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	Vcm			7.5	mV	RMS
Output Transition Time	Tr, Tf	28			ps	
Total Jitter	Tj			0.7	UIp-p	
Deterministic Jitter	DJ			0.4	UIp-p	
Eye Mask			See note			

Note:



## Block Diagram of Transceiver



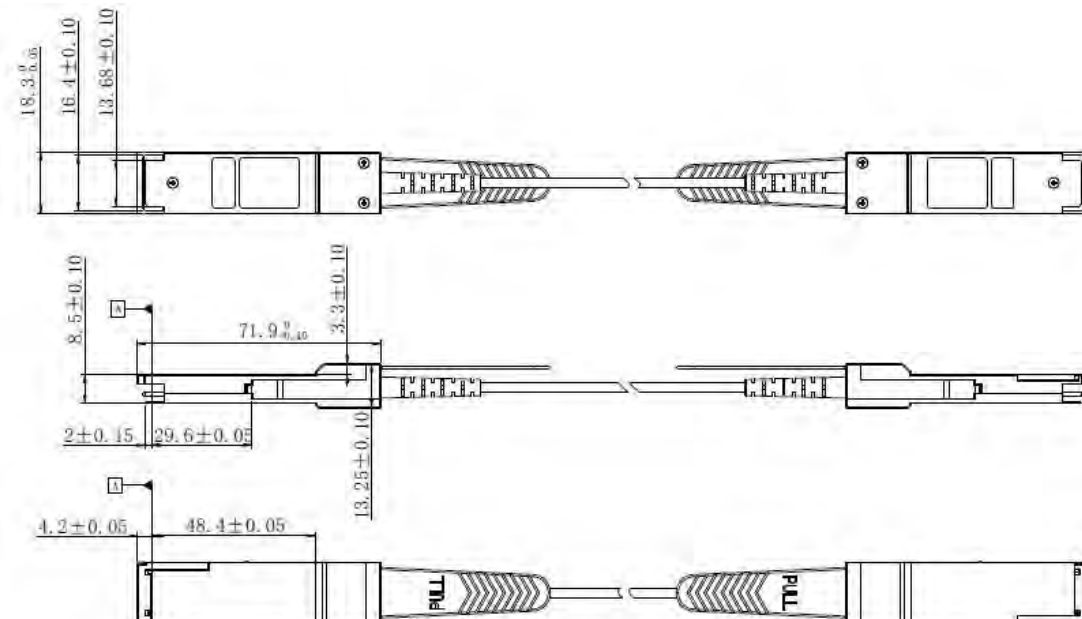
The QSFP AOC has miniature optical engine embedded into each end of the cable assembly. The engines interconnect 4 independent transmit/receive lanes.

A functional block diagram of the engine is shown in the above Figure. The transmitter sections consists of a 4- channel VCSEL array, a 4-channel input buffer and laser driver.

An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface.

The Receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

## Dimensions

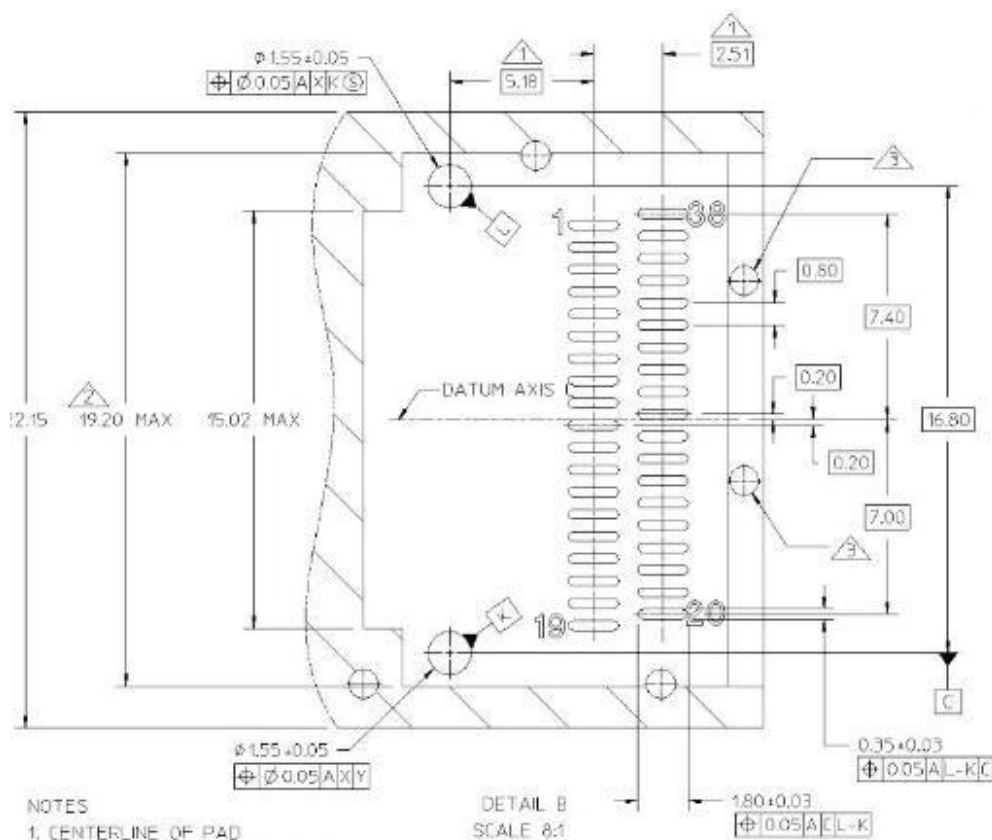
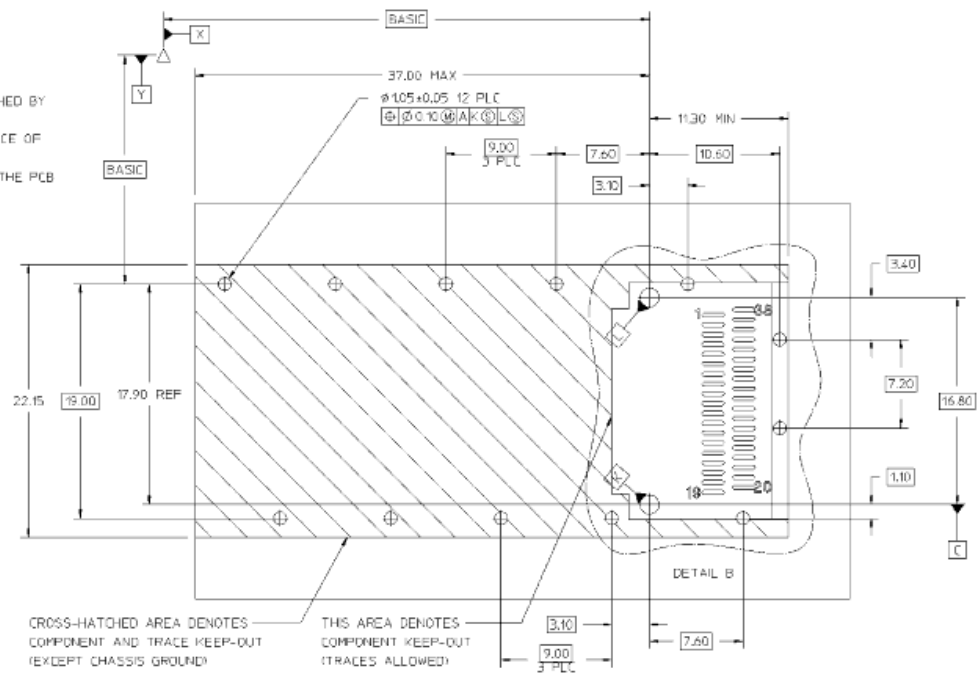


**ALL DIMENSIONS ARE  $\pm 0.2\text{mm}$  UNLESS OTHERWISE SPECIFIED**

**UNIT: mm**

## NOTES

1. DATUM X & Y ARE ESTABLISHED BY THE CUSTOMER'S FIDUCIAL
2. DATUM A IS THE TOP SURFACE OF THE HOST BOARD
3. LOCATION OF THE EDGE OF THE PCB IS APPLICATION SPECIFIC
4. FINISHED PTH HOLE SIZE



- ## NOTES

1. CENTERLINE OF PAD
2. SURFACE TRACES PERMITTED WITHIN THIS LENGTH
3. INDICATED HOLES ARE OPTIONAL

## Electrical Pad Layout

38	GND
37	TX1n
36	TX1p
35	GND
34	TX3n
33	TX3p
32	GND
31	LPMODE
30	VCC1
29	VCCTX
28	INTL
27	MODPRSL
26	GND
25	RX4p
24	RX4n
23	GND
22	RX2p
21	RX2n
20	GND

Top Side  
Viewed from Top

Card Edge

GND	1
TX2n	2
TX2p	3
GND	4
TX4n	5
TX4p	6
GND	7
ModSelL	8
ResetL	9
VCCRX	10
SCL	11
SDA	12
GND	13
RX3p	14
RX3n	15
GND	16
RX1p	17
RX1n	18
GND	19

Bottom Side  
Viewed from Bottom

## Pin Assignment

<i><b>PIN#</b></i>	<i><b>Symbol</b></i>	<i><b>Description</b></i>	<i><b>Remarks</b></i>
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	V <sub>cc</sub> RX	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	V <sub>cc</sub> TX	+3.3V Power Supply transmitter	
30	V <sub>cc1</sub>	+3.3V Power Supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	

## References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.
2. QSFP+ 10Gbs 4X PLUGGABLE TRANSCEIVER – SFF-8436