CFP-100G-LR4-C

CFP 1310 nm wavelength 100GbE Transceiver

CFP-100G-LR4-C Overview:

100GbE CFP-100G-LR4-C and ITU-T G.959.1 CFP-100G-LR4-C for 10km applications Dual Protocol Transceiver for 103.125 & 111.810 Gbit/s operation with LC connecter.

Product Features

- 100Gigabit Ethernet (100GbE) CFP-100G-LR4-C & ITU-T G.959.1 CFP-100G-LR4-C Dual Protocol Transceiver
- Compliant to IEEE 802.3ba CFP-100G-LR4-C [1] and ITU-T G.959.1 CFP-100G-LR4-C [2]
- 103.125 & 111.810 Gbit/s Dual Rate Capability
- 10.3125 Gbit/s x 10 channel Electrical Serial Interface (CAUI) [1] and 11.1810 Gbit/s x 10 channel Electrical Serial Interface (OTL4.10) [3]
- Transmission length up to 10 km [1][2]
- Compliant to CFP MSA [4]
- 1310 nm cooled EA-DFB LD for Optical light source
- PIN Photo detector for Optical receiver
- Low power consumption: 16 W max
- Operating Case Temperature: 0 to 70 deg C
- LC-Duplex Optical Receptacle
- Hot Z-Pluggable to 148-pin electrical connector
- Latching mechanism: Screw Latch
- MDIO Management Interface [5]
- Host lane and network lane loopback function supported

Applications

- Enterprise core aggregation and telecom/MSO optical transport
- IP switches/routers, Metropolitan Area Networks, DWDM systems and SAN applications
- 100GbE and OTN Optical transport applications

Part No.	Data Rate	Fiber	Distance	Interface	Temp.	DDMI
CFP-100G-LR4-C	100Gbps	SMF	10km	LC	0℃~+70℃	Yes

REFERENCE

[1] IEEE 802.3ba CFP-100G-LR4-C
[2] ITU-T G.959.1
[3] ITU-T G.709
[4] CFP MSA Hardware Specification, Rev. R1.4
[5] CFP MSA MDIO Specification, Rev. R1.4

DESCRIPTION

ProLabs's 100GbE transceiver module CFP-100G-LR4-C enables a dense-port and high-throughput solution in favor of its compact size and low power consumption. The CFP-100G-LR4-C modules can be used in various network applications, such as dense wavelength division multiplexing (DWDM) systems, metropolitan area network (MAN) systems, Internet Protocol (IP) switches and routers and Storage Area Network (SAN) applications. The maximum transmission length of CFP-100G-LR4-C is 10km [1][2].

The CFP-100G-LR4-C is a fully integrated 100Gbit/s optical transceiver module that consists of a 1310 nm wavelength cooled EA-DFB LD, Driver IC, PIN photo-diode, pre-amplifier, a 10:4 MUX with a clock generation circuit, a 4:10 DMUX with a clock and data recovery (CDR) circuit, and CAUI interface circuit.

Mechanical dimensions, connecters and footprint of CFP-100G-LR4-C conform to CFP MSA [4]. The module size is 82 mm x 144.75 mm x 13.6 mm and hot pluggable in Z-direction by 148-pin connector. The maximum power consumption is 16 W and power supply voltage is +3.3 V.

Example of a CFP-100G-LR4-C Transceiver

PERFORMANCE SPECIFICATIONS

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device.

Table 1 Absolute Maximum Ratings

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Supply Voltage	VCC	0	+3.6	V	+3.3 V
2	Storage Temperature	Tstr	-40	85	°C	
3	Optical Receiver Input	Pimax	-	+5.5	dBm	Average

Operating Environment

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 2 Operating Environment

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	VCC	3.2	3.3	3.4	V	
2	Power Supply Noise	Vrip			2 3	% %	DC – 1MHz 1 – 10MHz
3	Case Temperature	TC	0	25	70	°C	

Optical Characteristics

Table 3 Optical Characteristics for CFP-100G-LR4-C (Note1)

No.	Parameter		Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Channel data rate		f_{DC}		25.78125		Gbit/s	
2	Aggregate data rate		f_D		103.125		Gbit/s	IEEE 802.3ba
3	Signal speed variation from nominal		Δf_D	-100		+100	ppm	
4	Transmitter Center Wavelength							
		Lane 0	λ_{CT0}	1294.53		1296.59	nm	
		Lane 1	λ_{CT1}	1299.02		1301.09		
		Lane 2	λ_{CT2}	1303.54		1305.63		
		Lane 3	λ_{CT3}	1308.09		1310.19		
5	Optical Output Power in OMA		OMA	-1.3		+4.5	dBm	Note2
6	Average Optical Output Power of Off Transmitter		P_{off}			-30	dBm	
7	Optical Waveform		-		Figure 5			IEEE 802.3ba
8	Extinction Ratio		ER	4			dB	
9	Receiver Sensitivity in OMA		P_{minOMA}	-8.6		+4.5	dBm	
10	Stressed Receiver Sensitivity in OMA		$P_{minSOMA}$	-6.8			dBm	
11	Receive Power, each lane in OMA					+4.5	dBm	

Note 1: Data Rate; NRZ, Mark Ratio 50%, PRBS=2^{31}-1, $1x10^{-12}$ BER unless otherwise specified.

Note 2: $OMA=10\log_{10}[2P\{(A-1)/(A+1)\}]$, $A = 10^{(ER/10)}$, $P = 10^{(Pf/10)}$

Table 4 Optical Characteristics for CFP-100G-LR4-C (Note1)

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Channel data rate	f_{DC}		27.952493392		Gbit/s	
2	Aggregate data rate	f_D		111.809973568		Gbit/s	ITU-T G.709
3	Signal speed variation from nominal	□f_D	-20		+20	ppm	
4	Transmitter Center frequency						
	Lane 3		228.816	229	229.184	THz	
	Lane 2		229.616	229.8	229.984	THz	
	Lane 1		230.416	230.6	230.784	THz	
	Lane 0		231.216	231.4	231.584	THz	
5	Average Optical Power per lane		-2.5		+2.9	dBm	
	Average Optical Power total lane				+8.9	dBm	
	Channel Power Difference				5	dB	
6	Average Optical Output Power of Off Transmitter	P_{off}			-30	dBm	
7	Optical Waveform	-		Figure 5			ITU-T G.959.1
8	Extinction Ratio	ER	7			dB	
9	Mean Channel Input Power		-6.9/-8.8		+4/+2.9	dBm	Note 3
	Mean Total Input Power				+10/+8.9	dBm	Note 3
	Channel Power Difference				5.5	dB	
	Optical Path Penalty				1.5	dB	
10	Equivalent Sensitivity		-8.4/ -10.3			dBm	Note 2 Note 3
11	Receiver Reflectance per lane				-26	dB	

Note 1: Data Rate; NRZ, Mark Ratio 50%, PRBS=2^{31}-1, 1x10^{-12} BER unless otherwise specified.

Note 2: The Maximum bit error ratio for this application code of 1E-12 is only after error correction has been applied. The BER at optical input specified as Minimum equivalent sensitivity can therefore be 1.8E-4 without error correction.

Note 3: Two sets of specifications are defined depending on ER of input optical waveforms, the left set for ER between 4 dB and 7dB and the right set for ER of 7dB or higher.

Electrical Characteristics

Table 5 Power supply Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Current	ICC	-	-	10	A	Note 1
2	Supply Current @Low Power Mode	ICCL	-	-	0.6	A	
3	Power Consumption	Pw	-	-	16	W	
4	Power Consumption @Low Power Mode	Plow	-	-	2	W	

Note 1: Including in rush current. Maximum module current ramp rate is 50 mA /μs.

Table 6 3.3V LVCMOS level

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	VIH	2	-	VCC + 0.3	V	
2	Input Low Voltage	VIL	-0.3	-	0.8	V	
3	Input Leakage Current	IIN	-10	-	+10	μA	
4	Output High Voltage	VOH	VCC – 0.2	-	-	V	I_{OH}=-100μA
5	Output Low Voltage	VOL	-	-	0.2	V	I_{OL}=100μA
6	Minimum Pulse Width of Control Pin Signal	t_CNTL	100				μs

Table 7 1.2VLVCMOS level

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Input High Voltage	VIH	0.84	-	1.5	V	
2	Input Low Voltage	VIL	-0.3	-	0.36	V	
3	Input Leakage Current	IIN	-100	-	+100	µA	
4	Output High Voltage	VOH	1.0	-	1.5	V	
5	Output Low Voltage	VOL	-0.3	-	0.2	V	
6	Output High Current	IOH	-	-	-4	mA	
7	Output Low Current	IOL	+4	-	-	mA	
8	Input capacitance	Ci	-	-	10	pF	

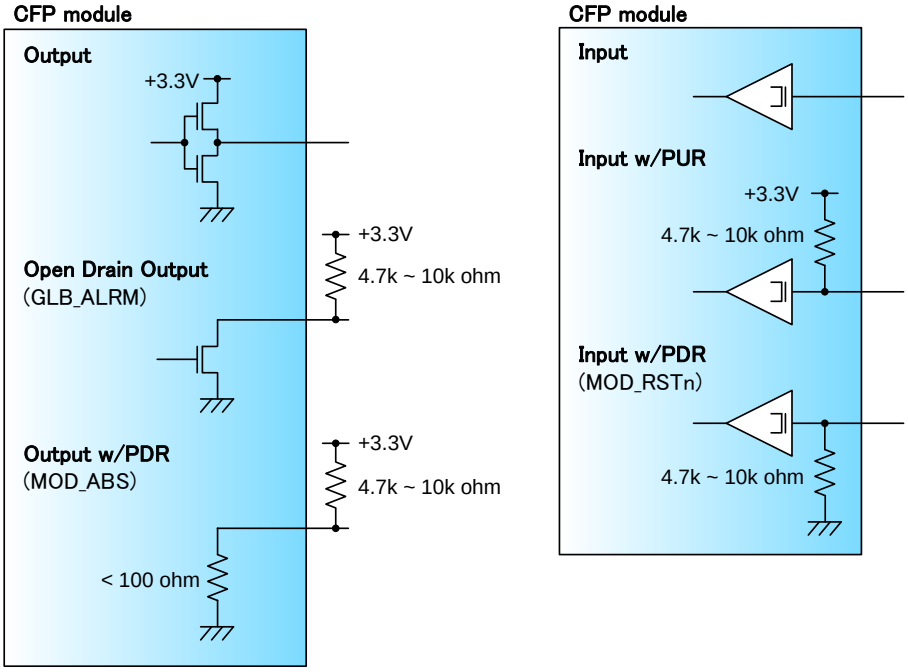


Figure 1 3.3V LVCMOS Interface

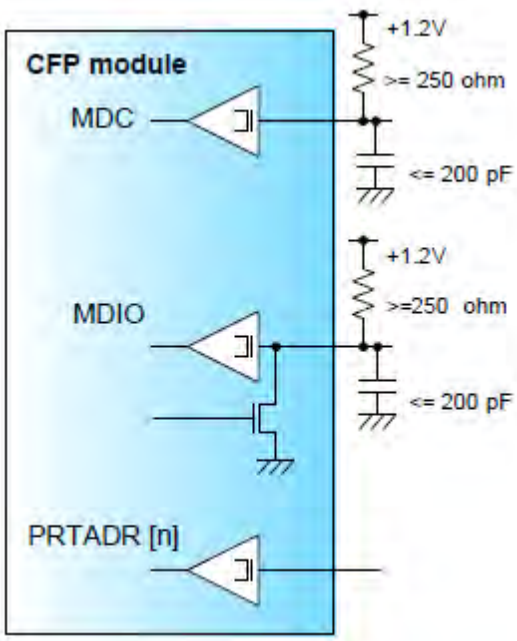
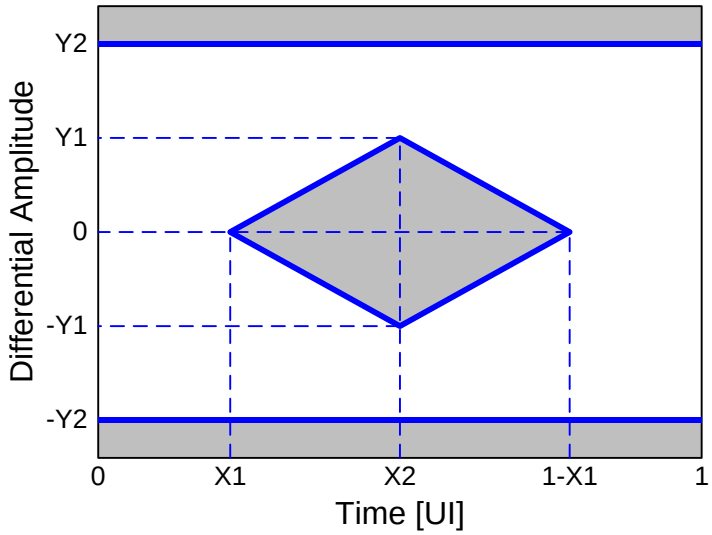


Figure 2 MDIO Interface

Table 8 CAUI Input Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Differential Input Voltage			Figure 3.		Vpp	
2	Input AC Common Mode Voltage				20	mVRMS	
3	Input Rise and Fall time		24			ps	20~80%
4	Total Jitter				0.62	UI	
5	non-EQ Jitter (Tj-ISI)				0.42	UI	
6	Eye Mask			Figure 3.			

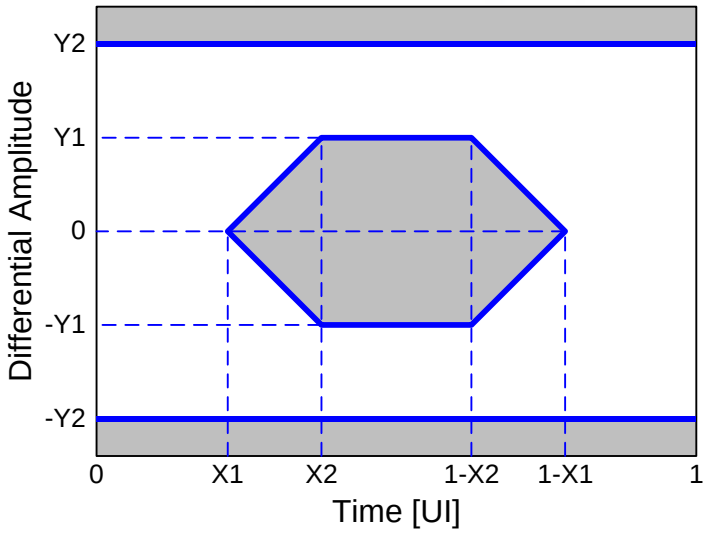


X1	X2	Y1	Y2
0.31	0.5	42.5 mV	425 mV

Figure 3 Mask of CAUI Input Eye Diagram

Table 9 CAUI Output Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Differential Output Voltage				0.76	Vpp	
2	Output AC Common Mode Voltage				15	mVRMS	
3	Output Rise and Fall time		24			ps	20~80%
4	Total Jitter				0.4	UI	
5	Eye Mask			Figure 4.			



X1	X2	Y1	Y2
0.2	0.5	136 mV	380 mV

Figure 4 Mask of CAUI Output Eye Diagram

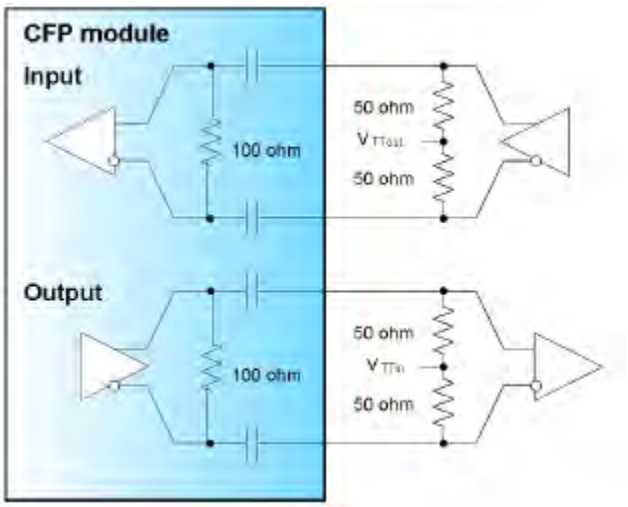
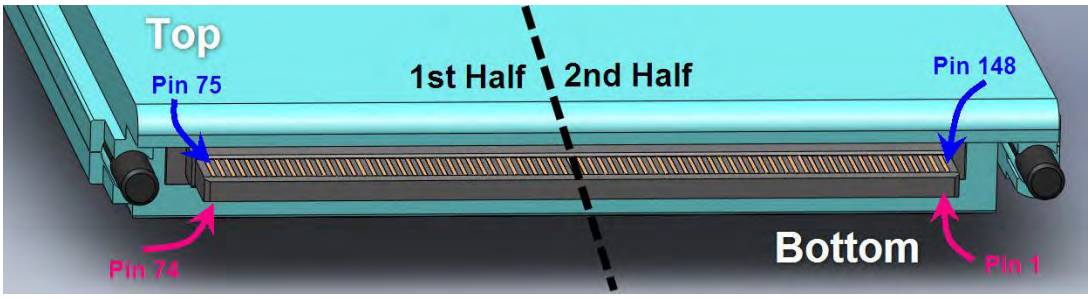


Figure 5 High speed I/O for Data and Clocks

CFP-100G-LR4 Transceiver Pin-Out



	Top Row (2nd Half)		Bottom Row (2nd Half)
148	GND	1	GND
147	REFCLKn	2	GND
146	REFCLKp	3	GND
145	GND	4	GND
144	No Connect	5	GND
143	No Connect	6	VCC
142	GND	7	VCC
141	TX9n	8	VCC
140	TX9p	9	VCC
139	GND	10	VCC
138	TX8n	11	VCC
137	TX8p	12	VCC
136	GND	13	VCC
135	TX7n	14	VCC
134	TX7p	15	VCC
133	GND	16	GND
132	TX6n	17	GND
131	TX6p	18	GND
130	GND	19	GND
129	TX5n	20	GND
128	TX5p	21	VND_IO_A
127	GND	22	VND_IO_B
126	TX4n	23	GND
125	TX4p	24	TX_MCLKn
124	GND	25	TX_MCLKp
123	TX3n	26	GND
122	TX3p	27	VND_IO_C
121	GND	28	VND_IO_D
120	TX2n	29	VND_IO_E
119	TX2p	30	PRG_CNTL1
118	GND	31	PRG_CNTL2
117	TX1n	32	PRG_CNTL3
116	TX1p	33	PRG_ALRM1
115	GND	34	PRG_ALRM2
114	TX0n	35	PRG_ALRM3
113	TX0p	36	TX_DIS
112	GND	37	MOD_LOPWR

	Top Row (1st Half)		Bottom Row (1st Half)
111	GND	38	MOD_ABS
110	No Connect	39	MOD_RSTn
109	No Connect	40	RX_LOS
108	GND	41	GLB_ALRMn
107	RX9n	42	PRTADR4
106	RX9p	43	PRTADR3
105	GND	44	PRTADR2
104	RX8n	45	PRTADR1
103	RX8p	46	PRTADR0
102	GND	47	MDIO
101	RX7n	48	MDC
100	RX7p	49	GND
99	GND	50	VND_IO_F
98	RX6n	51	VND_IO_G
97	RX6p	52	GND
96	GND	53	VND_IO_H
95	RX5n	54	VND_IO_J
94	RX5p	55	GND
93	GND	56	GND
92	RX4n	57	GND
91	RX4p	58	GND
90	GND	59	GND
89	RX3n	60	VCC
88	RX3p	61	VCC
87	GND	62	VCC
86	RX2n	63	VCC
85	RX2p	64	VCC
84	GND	65	VCC
83	RX1n	66	VCC
82	RX1p	67	VCC
81	GND	68	VCC
80	RX0n	69	VCC
79	RX0p	70	GND
78	GND	71	GND
77	RX_MCLKn	72	GND
76	RX_MCLKp	73	GND
75	GND	74	GND

Figure 6 Pin Configuration

Table 10 Pin Description

PIN #	NAME	I/O	Logic	Description
1	GND			
2	GND			
3	GND			
4	GND			
5	GND			
6	VCC			3.3V Module Supply Voltage
7	VCC			
8	VCC			
9	VCC			
10	VCC			
11	VCC			
12	VCC			
13	VCC			
14	VCC			
15	VCC			
16	GND			
17	GND			
18	GND			
19	GND			
20	GND			
21	VND_IO_A	I/O		Vendor I/O A. Do not connect any signal.
22	VND_IO_B	I/O		Vendor I/O B. Do not connect any signal.
23	GND			
24	TXMCLK OUT N	O	CML	For optical waveform testing. Not for normal use.
25	TXMCLK OUT P	O	CML	
26	GND			
27	VND_IO_C	I/O		Vendor I/O C. Do not connect any signal.
28	VND_IO_D	I/O		Vendor I/O D. Do not connect any signal.
29	VND_IO_E	I/O		Vendor I/O E. Do not connect any signal.
30	PRG_CNTL1	I	LVCMOS w/ PUR	Programmable Control 1 set over MDIO, Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	PRG_CNTL2	I	LVCMOS w/ PUR	Programmable Control 2 set over MDIO, Default: Hardware Interlock LSB, "00": <8W, "01": <16W, "10": <24W, "11" or NC: ≤32W = not used
32	PRG_CNTL3	I	LVCMOS w/ PUR	Programmable Control 3 set over MDIO, Default: Hardware Interlock MSB, "00": <8W, "01": <16W, "10": <24W, "11" or NC: ≤32W = not used
33	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not high powered up
34	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, "1": Ready, "0": not Ready.
35	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, "1": Fault, "0": No Fault
36	TX_DIS	I	LVCMOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LVCMOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled

PIN #	NAME	I/O	Logic	Description
38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LVCMOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	GLB_ALRMn	O	LVCMOS (Open Drain)	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition
42	PRTADR4	I	1.2V CMOS	MDIO port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Vendor I/O F. Do not connect any signal.
51	VND_IO_G	I/O		Vendor I/O G. Do not connect any signal.
52	GND			
53	VND_IO_H	I/O		Vendor I/O H. Do not connect any signal.
54	VND_IO_J	I/O		Vendor I/O J. Do not connect any signal.
55	GND			
56	GND			
57	GND			
58	GND			
59	GND			
60	VCC			3.3V Module Supply Voltage
61	VCC			
62	VCC			
63	VCC			
64	VCC			
65	VCC			
66	VCC			
67	VCC			
68	VCC			
69	VCC			
70	GND			
71	GND			
72	GND			
73	GND			
74	GND			

PIN #	NAME	I/O	Logic	Description
75	GND			
76	RX_MCLKp	O	CML	For optical waveform testing. Not for normal use.
77	RX_MCLKn	O	CML	
78	GND			
79	RX0p	O	CML	Received data output of CAUI ch0.
80	RX0n	O	CML	
81	GND			
82	RX1p	O	CML	Received data output of CAUI ch1.
83	RX1n	O	CML	
84	GND			
85	RX2p	O	CML	Received data output of CAUI ch2.
86	RX2n	O	CML	
87	GND			
88	RX3p	O	CML	Received data output of CAUI ch3.
89	RX3n	O	CML	
90	GND			
91	RX4p	O	CML	Received data output of CAUI ch4.
92	RX4n	O	CML	
93	GND			
94	RX5p	O	CML	Received data output of CAUI ch5.
95	RX5n	O	CML	
96	GND			
97	RX6p	O	CML	Received data output of CAUI ch6.
98	RX6n	O	CML	
99	GND			
100	RX7p	O	CML	Received data output of CAUI ch7.
101	RX7n	O	CML	
102	GND			
103	RX8p	O	CML	Received data output of CAUI ch8.
104	RX8n	O	CML	
105	GND			
106	RX9p	O	CML	Received data output of CAUI ch9.
107	RX9n	O	CML	
108	GND			
109	No Connect			No internal connection. Do not connect any signal.
110	No Connect			
111	GND			

PIN #	NAME	I/O	Logic	Description
112	GND			
113	TX0p	I	CML	Transmit data input of CAUI ch0.
114	TX0n	I	CML	
115	GND			
116	TX1p	I	CML	Transmit data input of CAUI ch1.
117	TX1n	I	CML	
118	GND			
119	TX2p	I	CML	Transmit data input of CAUI ch2.
120	TX2n	I	CML	
121	GND			
122	TX3p	I	CML	Transmit data input of CAUI ch3.
123	TX3n	I	CML	
124	GND			
125	TX4p	I	CML	Transmit data input of CAUI ch4.
126	TX4n	I	CML	
127	GND			
128	TX5p	I	CML	Transmit data input of CAUI ch5.
129	TX5n	I	CML	
130	GND			
131	TX6p	I	CML	Transmit data input of CAUI ch6.
132	TX6n	I	CML	
133	GND			
134	TX7p	I	CML	Transmit data input of CAUI ch7.
135	TX7n	I	CML	
136	GND			
137	TX8p	I	CML	Transmit data input of CAUI ch8.
138	TX8n	I	CML	
139	GND			
140	TX9p	I	CML	Transmit data input of CAUI ch9.
141	TX9n	I	CML	
142	GND			
143	No Connect			No internal connection. Do not connect any signal.
144	No Connect			
145	GND			
146	REFCLKp	I	CML	Reference Clock Input.
147	REFCLKn	I	CML	
148	GND			

Mechanical Dimension

- All Units in mm

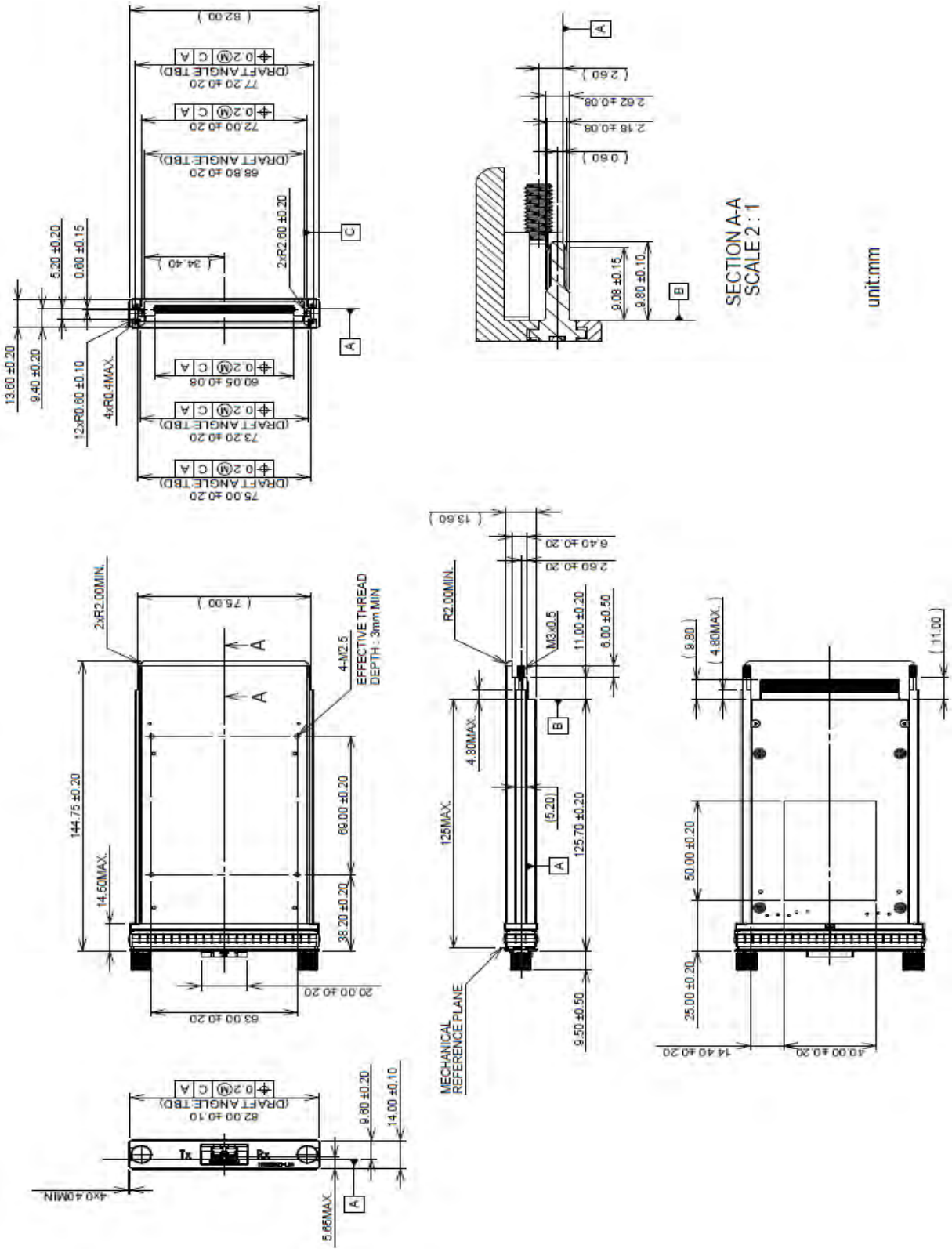


Figure 7 Mechanical dimensions of CFP-100G-LR4-C

USER INFORMATION

Handling Precautions

CAUTION: Take proper electrostatic-discharge (ESD) precautions while handling these devices. These devices are sensitive to ESD.

EMI Compliance

This product meets Electromagnetic Interference (EMI) specifications of following standards.

Table 11 EMI Compliance

No.	Standards	Criteria	Remarks
1	FCC	Class B	Target
2	EN55002	Class B	Target

Laser Safety

This product is complied with IEC 60825-1 as Class 1 and with FDA 21 CFR as Class I laser product.